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Extended Topology for Boost DC-DC Converter

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***Abstract*—In this paper, a new structure for non-isolated boost dc-dc converter is proposed. The proposed converter generates higher voltage gain than some conventional non-isolated boost dc-dc converters. In this paper, the voltage and current equations of the elements and voltage gain in continuous conduction mode (CCM) and discontinuous conduction mode (DCM) are extracted. Then, the critical inductance converter is extracted and the current stresses in the switches are calculated. To achieve high voltage gain, a generalized structure based on the proposed structure generates for dc-dc converters. Meanwhile, the root mean square current relations of devices are obtained for extended structure. Finally, to confirm the accuracy of the simulation results on software PSCAD/EMTDC and experimental results by laboratory prototype are used.**

***Index Terms*—Dc-dc converter, non-isolated boost converter, critical inductance, voltage gain.**

Nomenclature

$v_{L1,1}$, $v_{L1,2}$, $v_{L1,3}$, $v_{L1,4}$, $v_{L2,1}$, $v_{L2,2}$, $v_{L2,4}$, $v_{C1,1}$, $v_{C1,2}$, $v_{C1,3}$, $v_{D1,1}$, $v_{D1,2}$, $v_{D1,4}$, $v_{D2,1}$, $v_{D2,2}$, $v_{Do,2}$, $v_{Do,3}$, $v_{Do,4}$, $i_{L1,1}$, $i_{L1,2}$, $i_{L1,3}$, $i_{L1,4}$, $i_{L2,1}$, $i_{L2,2}$, $i_{L2,3}$, $i_{L2,4}$, $i_{C1,1}$, $i_{C1,2}$, $i_{C1,3}$, $i_{Co,1}$, $i_{Co,2}$, $i_{D1,2}$, $i_{D1,3}$, $i_{D2,2}$, $i_{D2,3}$, $i_{Do,1}$	The current (i) and voltage (v) of the element shown in the subtitle at a specified time interval. The subtitle 1 and 2 show T_{on} and T_{off} in CCM, respectively. Also, the subtitle 1, 2, 3 and 4 indicate the time intervals of (t_0, t_1), (t_1, t_2), (t_2, t_3) and (t_3, t_4) in DCM, respectively.
Δi_{L1}, Δi_{L2}	The inductors current ripple.
v_{C1}, v_{Co}	The capacitors average voltage.
I_o, V_o, I_i, V_i	The load (o) and source (i) average parameters.
K, B_{ac}^{β}, W_{tfe}, α, β	Inductor core parameters
C_{OSS}, $Q_{rr,BD}$, r_{BD}, I_{BD}, V_{BF}	Switch parameters
Q_{rr}, r_D, I_D, V_F	Diode parameters

I. Introduction

Nowadays, dc-dc converters are used in many ways such as hybrid electric vehicles, renewable energy sources such as wind turbines generators, solar cells and fuel cells, medical equipment and servo-motors, industrial circuits and power factor correction (PFC), telecommunication systems and air and space industry and portable electrical equipment such as portable computers and mobile phones [1-2]. The converter switching control is done by pulse width modulation (PWM) and switching frequency change [1-2]. The positive and negative output voltages with respect to input ground can be generated by both of these switching methods. Converters that switching control is performed by PWM are classified in non-isolated dc-dc converters such as buck, boost, buck-boost, CUK, and SEPIC converters and isolated dc-dc converters such as fly-back, forward, half-bridge, full-bridge and push-pull [3-4]. Non-isolated converters do not include high frequency transformer in their structure. As a result, they have less size and low cost and are easier to control. Among non-isolated converters, those that have greater fixed output voltage than the input voltage are acceptable. Direct connection of inductor at the input and lower output capacitance and size of output filter, switch protection against overvoltage and electromagnetic interference (EMI), lower stress on the elements, more transient response, efficiency and high power density are features of these converters. Thus, the dc-dc converter are used in many dc-dc applications of renewable energy sources such as wind turbine generators [5], solar cells [6] and fuel cells [7], improving power quality in industrial circuits and PFC [8-9] and LED devices [10].

Introducing new structure [11-12], analyzing performance [13] and stability analysis, modeling, control and, designs of controller [14] for these converters are topics of interest to researchers. In [11-12], structures based on buck-boost converters are proposed in order to achieve maximum voltage with minimum switches. To enhance the conventional boost converter in output voltage, different structures and techniques including capacitor switching technique (SC) [15-17] and combination with other dc-dc converters [18], and voltage lift (VL) technique [19-20] are introduced. In SC technique [15-17], by incorporating several switches and capacitors with minimum inductor achieving a higher output voltage than the input voltage is easily possible. However, this combination increases the complexity due to number of power switches and increases the current stress of switching. To fix the current stress, coupled inductor is used which increases the size and cost of the converter and is not very popular. In [18], series and parallel combinations of converters with other dc-dc converter in order to achieve a higher output voltage than input, particularly for renewable energy applications have been investigated. Because of the increased size, cost, complexity of control it was not very interesting to researchers. Eventually, VL technique based on inductor and capacitor elements feature for energy storage and reducing voltage stress of switch was introduced [19-20] and by implementing it, new structures for non-isolated boost converter were presented. In [21-23], new structures to enhance the output voltage by using the least elements based on VL techniques were proposed and compared with other

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proposed structures. Meanwhile, the new structure based on one switch and two switches were introduced in [24] and [25], respectively.

In this paper, a new structure for non-isolated dc-dc boost converters using VL technique has been proposed that the higher voltage is achieved. The output voltage of the proposed converter is negative with respect to input ground. In this paper, performance of non-isolated boost converter was analyzed in detail in CCM and DCM and inductors and capacitors voltage and current relations are extracted, then gains of current and voltage for CCM and DCM are calculated and are compared with non-isolated conventional dc- dc converters. Furthermore, the critical inductance between CCM and DCM is calculated and stresses of switches are extracted. Then generalized structure is proposed for achieving higher voltage gain. Finally, the accuracy of offered theory is reaffirmed by simulation results in PSCAD/EMTDC software and experimental results by using laboratory prototype.

II. The Proposed Structure

The proposed converter structure is shown in Fig. 1. As can be seen, two power switches, two inductors, three diodes and two capacitors are used. In the proposed structure, the voltage boosting stage consists of one inductor, one capacitor, and two diodes. The operating of switches is controlled by PWM technique and opposes each other. To simplify the analysis, the following assumptions are considered, a) converter is in steady state, so output voltage V_o is constant, b) the capacitors C_1 and C_o are large enough and therefore their voltage in each switching period remain unchanged, c) All switches and diodes are ideal. In the following, equations of the current and voltage of each element in CCM and DCM are discussed.

A. Analysis of Proposed Converter in CCM

At T_{on} when the switch S_1 is turned on and the switch S_2 is turned off, the inductor L_1 is directly connected to V_i. In this case, the current of inductor L_1 is linearly increased from its minimum value (I_{LV1}) to its maximum value (I_{LP1}). Thus, its stored energy is gradually increased. Also, the D_o diode is directly biased, and the diodes of D_1 and D_2 are reversely biased. Therefore, the inductor L_2 and capacitor C_1 are connected in series and provided the currents of the load and charge of capacitor C_o. Also, the stored energy of the inductor L_2 and capacitor C_1 are gradually decreased.

At T_{off} when the switch S_1 is turned off and the switch S_2 is turned on, the diodes of D_1 and D_2 are directly biased and the D_o diode is reversely biased, hence, the inductor L_1 is connected to the inductor L_2 and capacitor C_1. As a result, the stored energy of inductor L_1 is gradually decreased and its current is reduced from its maximum value to its minimum value gradually. Also, the stored energy of the inductor L_2 and capacitor C_1 are gradually increased, therefore the passing current through inductor L_2 is gradually increased from its maximum value to its minimum value. In addition, the voltage of capacitor C_1 is increased from its minimum value to its maximum value. Here, the capacitor C_o discharge current provided the load current as a result its stored energy is gradually reduced and its voltage is reduced from its maximum value to its minimum value.

The voltage and current waveforms of each elements of the proposed converter in CCM is shown in Fig. 2.

By applying KVL in the time interval of T_{on}, we have:

$$V_i = v_{L1,1} = L_1 \frac{di_{L1,1}}{dt} = L_1 \frac{\Delta i_{L1}}{T_{on}} \quad (1)$$

By applying KVL in the time interval of T_{off}, we have:

$$V_i - v_{C1,2} = v_{L1,2} = L_1 \frac{di_{L1,2}}{dt} = -L_1 \frac{\Delta i_{L1}}{T_{off}} \quad (2)$$

Applying the voltage-balancing rule for inductor L_1 and defining new time offset for T_{off}, considering (1) and (2) and by defining duty cycle $(D = T_{on}/T)$, we have:

$$v_{C1,2} = \frac{1}{1-D} V_i = v_{C1,1} = v_{C1} \quad (3)$$

At T_{on} and T_{off}, we have the following equations:

$$i_{C1,1} = -(i_{Co,1} + I_o) = i_{L2,1} \quad (4)$$

$$i_{C1,2} = i_{L1,2} - i_{L2,2} \quad (5)$$

By applying KVL in the time interval of T_{on}, we get:

$$v_{C1,1} - V_o = v_{L2,1} = L_2 \frac{di_{L2,1}}{dt} = -L_2 \frac{\Delta i_{L2}}{T_{on}} \quad (6)$$

At T_{off}, the voltage of inductor L_2 is obtained:

$$V_i - v_{L1,2} = v_{L2,2} = L_2 \frac{di_{L2,2}}{dt} = L_2 \frac{\Delta i_{L2}}{T_{off}} \quad (7)$$

The average voltage of capacitor C_o is as follows:

$$v_{Co} = V_o \quad (8)$$

The current of capacitor C_o is as follows:

$$i_{Co,1} = i_{C1,1} - I_o \quad (9)$$

$$i_{Co,2} = -I_o \quad (10)$$

The below relations are obtained for the diodes:

$$v_{D1,1} = -v_{C1,1} \quad (11)$$

$$i_{D1,2} = i_{C1,2} + i_{L2,2} \quad (12)$$

$$v_{D2,1} = 0 \quad (13)$$

$$i_{D2,2} = i_{L2,2} \quad (14)$$

$$i_{Do,1} = i_{Co,1} + I_o \quad (15)$$

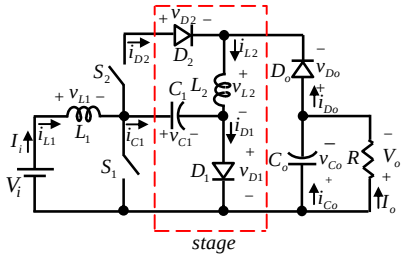

Fig. 1. Proposed converter

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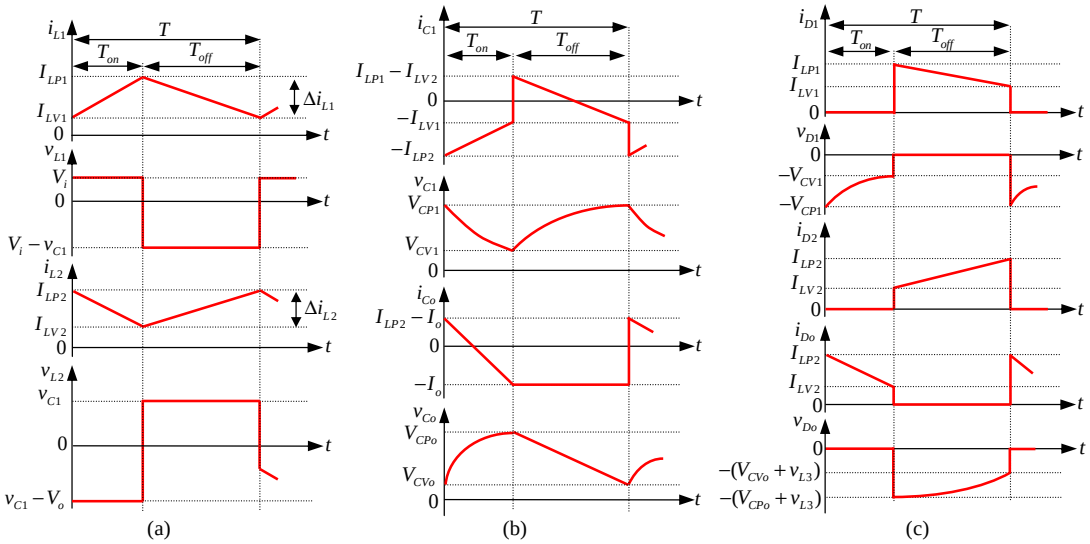

Fig. 2. Key waveforms in CCM for; (a) inductors L_1 and L_2; (b) capacitors C_1 and C_o; (c) diodes D_1, D_2 and D_o

$$v_{Do,2} = -(v_{Co,2} + v_{L2,2}) \tag{16}$$

By applying voltage-balancing rule for inductor L_2, replacing (6), (7) and (3), the voltage gain of proposed converter in CCM is obtained as follows:

$$\frac{V_o}{V_i} = -\frac{1}{D(1-D)} \tag{17}$$

Assuming no losses, we have:

$$\frac{I_o}{I_i} = -D(1-D) \tag{18}$$

Assuming the pure resistance load (R), we have:

$$I_o = -\frac{V_i}{D(1-D)R} \tag{19}$$

A.1. Comparison of The Proposed Converter with Conventional Converters

Summary of results of the comparison between the proposed boost converter and other conventional boost converters is presented in Table I. The curve of voltage gain for proposed converter in CCM for different values of D with same input voltage is shown Fig. 3(a) and is compared to presented converters in [21] and [24]. As can be seen, for same number of elements and switches compared to [21], higher and acceptable voltage gain is achieved by the proposed converter. Of course, the voltage gain of the proposed converter is better than [24].

The other two switches converter was presented in [15] (two switched capacitors with diode-capacitor stages). Although the proposed converter has one more inductor in its structure in comparison with the presented structure in [15] (two switched capacitors with diode-capacitor stages), but the number of capacitors and diodes of the studied structure in [15] is more than the proposed converter. Of course, when the proposed converter has been generalized with only two switches to n-stages, the number of used switches in the proposed structure will be its features. From the point of view of the number of elements, the proposed converter has one more diode compared to cascaded boost converter [23] whereas they have same voltage gain. Then, it can be noted that the proposed converter and cascaded boost converter have almost same cost and size. The total voltage and current stress of the proposed converter are compared with the presented structure in [21] and cascaded boost converter in [23] in order to show more features of the proposed converter. It should be noted that the presented converter in [23] was special state of the conventional cascaded boost converter by limitation in increasing D. In [23], switching pattern which is used for the conventional cascade boost converter as complementary, then, one of the converters could not operate with duty cycle higher than 0.5. As a result, the voltage gain in [23] has limited.

TABLE I
THE COMPARISON BETWEEN DIFFERENT BOOST CONVERTERS

Number of	Switch	Inductor	Capacitor	Diode	Voltage gain in CCM
Conventional boost converter	1	1	1	1	$\frac{1}{1-D}$
Presented in [21]	1	2	3	3	$\frac{1+D}{1-D}$
Presented in [22]	2	3	3	4	$\frac{2}{D(1-D)}$
Presented in [23]	2	2	2	2	$\frac{1}{D(1-D)}$
Presented in [24]	2	1	3	2	$1+D$
Presented in [25]	1	2	5	6	$\frac{n(3D+2)+(2-D)}{2(1-D)^2}$ n=turn ratio
Proposed topology n=1	2	2	2	3	$\frac{1}{D(1-D)}$

This comparison is done by considering same conditions V_i, D and f (such as $V_i = 12V$, $D = 30\% - 50\%$, $f = 10kHz$). The results of comparison are shown in Figs. 3(b) and 3(c). As illustrated in Fig. 3(b), the total voltage stress of the proposed converter is less than [21] and is near to

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[23]. Also, the total current stress of the presented converter in [21] is more than the total current stress of the proposed converter and [23]. It can be note that the total stress of the proposed converter is approximately equal to [23]. In [25], a single switch boost dc-dc converter with one coupled inductor has been introduced. Although, the presented structure provided suitable voltage gain but its number of elements is more than the proposed converter.

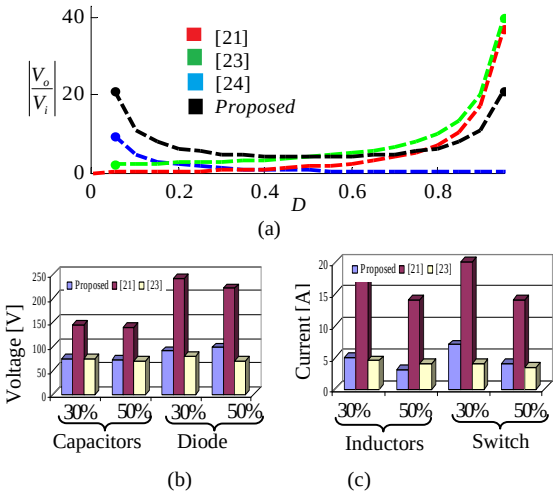

Fig. 3. (a) The curve of voltage gain variation for the proposed converter and other conventional converters; (b) total voltage stress comparison; (c) total current stress comparison

B. *Analysis of Proposed Converter in DCM*

At $(t_0,\ t_1)$ when the switch S_1 is turned on and the switch S_2 is turned off, the inductor L_1 is directly connected to V_i. During this time interval, the current of inductor L_1 is linearly increased from minimum, so its stored energy is gradually increased. Also, the diodes of D_1 and D_2 are directly biased and the D_o diode is reversely biased. So, the inductor L_2 and capacitor C_1 are connected in series and provided the load current and charge current of capacitor C_o. Then, the current of inductor L_2 and the voltage of capacitor C_1 are gradually decreased and as a results their stored energy are decreased. Meanwhile, the stored energy and voltage of capacitor C_o is increased to its maximum value.

At $(t_1,\ t_2)$ when the switch S_1 is turned on and the switch S_2 is turned off, the inductor L_1 is still connected directly to V_i and its current is linearly increased to its maximum value. During this time interval, the current of inductor L_2 is zero, as a result, the diodes of D_1, D_2 and D_o are reversely biased and the voltage of capacitor C_1 and its stored energy remains unchanged. Also, the load current provided by the discharge current of capacitor C_o and as the result, its voltage and stored energy is gradually decreased.

At $(t_2,\ t_3)$ when the switch S_1 is turned off and the switch S_2 is turned on, the diodes of D_1 and D_2 are directly biased and the D_o diode is reversely biased as a result the inductor L_1 is connected to the parallel combination of the inductor L_2 and capacitance C_1. Then, the stored energy and current of inductor L_1 are gradually decreased to its minimum and the stored energy of the inductor L_2 and capacitor C_1 are gradually increased. In addition, the load current is supplied by capacitor C_o discharge current, and as the result the stored energy and voltage of capacitor C_o are gradually reduced.

At $(t_3,\ t_4)$ when the switch S_1 is turned off and the switch S_2 is turned on, the current of inductor L_1 is zero and its stored energy is zero. As a result, the diodes of D_1, D_2 and D_o are reversely biased. In this time interval, the inductor L_2 and capacitor C_1 are in parallel. During in this time interval, the load current is provided by the discharge current of capacitor C_o, therefore its voltage and stored energy is reduced to minimum. The voltage and current waveforms of each elements of proposed converter in DCM is shown in Fig. 4. By applying KVL at $(t_0,\ t_2)$, we have:

$$V_i = v_{L1,2} = L_1 \frac{di_{L1,2}}{dt} = L_1 \frac{\Delta i_{L1}}{\Delta t} \tag{20}$$

At $(t_2,\ t_3)$, the voltage of inductor L_1 equals to:

$$V_i - v_{C1,3} = v_{L1,3} = L_1 \frac{di_{L1,3}}{dt} = -L_1 \frac{\Delta i_{L1}}{\Delta t} \tag{21}$$

At $(t_3,\ t_4)$, we get:

$$i_{L1,4} = 0 \tag{22}$$

$$v_{L1,4} = 0 \tag{23}$$

Different time intervals in DCM are defined as follows:

$$D_1' = \frac{t_1 - t_0}{T} \tag{24}$$

$$D_2' = \frac{t_2 - t_1}{T} \tag{25}$$

$$D_3' = \frac{t_3 - t_2}{T} \tag{26}$$

$$D_4' = \frac{t_4 - t_3}{T} \tag{27}$$

By applying voltage-balancing rule for L_1, considering (20), (21) and (23), defining duty cycle in DCM $(D' = D_1' + D_2')$ and simplifying, we get:

$$v_{C1,3} = \frac{D' + D_3'}{D_3'} V_i = v_{C1} \tag{28}$$

At $(t_0,\ t_1)$ and $(t_2,\ t_3)$, we have the following equation:

$$i_{C1,1} = -i_{L2,1} \tag{29}$$

$$i_{C1,3} = i_{L1,3} - i_{L2,3} \tag{30}$$

By applying KVL at $(t_0,\ t_1)$, we have:

$$v_{C1,1} - V_o = v_{L2,1} = L_2 \frac{di_{L2,1}}{dt} = -L_2 \frac{\Delta i_{L2}}{\Delta t} \tag{31}$$

At $(t_1,\ t_2)$, it is resulted:

$$i_{L2,2} = 0 \tag{32}$$

$$v_{L2,2} = 0 \tag{33}$$

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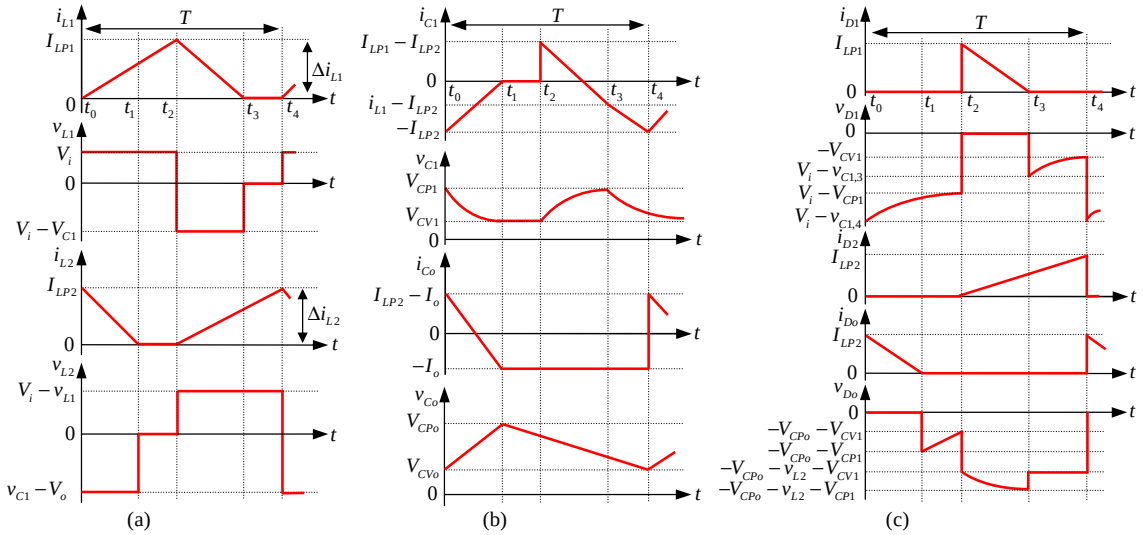

Fig. 4. Key waveforms in DCM for; (a) inductors L_1 and L_2; (b) capacitors C_1 and C_o; (c) diodes D_1, D_2 and D_o

The voltage of inductor L_2 at $(t_2,\ t_4)$ equals to:

$$V_i - v_{L1,4} = v_{L2,4} = L_2 \frac{di_{L2,4}}{dt} = L_2 \frac{\Delta i_{L2}}{\Delta t} \tag{34}$$

The average voltage of capacitor C_o is as follows:

$$v_{Co} = V_o \tag{35}$$

The current of capacitor C_o at $(t_0,\ t_1)$ and $(t_1,\ t_4)$ equal to, respectively:

$$i_{Co,1} = i_{C1,1} - I_o \tag{36}$$

$$i_{Co,4} = -I_o \tag{37}$$

The voltage and current of the diodes are equal to:

$$v_{D1,2} = -v_{C1,2} \tag{38}$$

$$v_{D1,4} = V_i - v_{C1,4} \tag{39}$$

$$i_{D1,3} = i_{C1,3} + i_{L2,3} \tag{40}$$

$$v_{D2,2} = 0 \tag{41}$$

$$i_{D2,3} = i_{L2,3} \tag{41}$$

$$i_{Do,1} = i_{Co,1} + I_o = i_{L2,1} \tag{43}$$

$$v_{Do,2} = v_{C1,2} - v_{L2,2} - V_o \tag{44}$$

$$v_{Do,3} = -(v_{L2,3} + V_o) \tag{45}$$

$$v_{Do,4} = v_{C1,4} - v_{L2,4} - V_i - V_o \tag{46}$$

From (31), (33) and (34), the voltage gain of proposed converter in DCM is as follows:

$$\frac{V_o}{V_i} = -\frac{(D_1' + D_2' + D_3')(D_1' + D_3' + D_4')}{D_1' D_3'} \tag{47}$$

By considering no losses, we get:

$$\frac{I_o}{I_i} = -\frac{D_1' D_3'}{(D_1' + D_2' + D_3')(D_1' + D_3' + D_4')} \tag{48}$$

By assuming pure resistance load (R), we have:

$$I_o = -\frac{(D_1' + D_2' + D_3')(D_1' + D_3' + D_4')}{D_1' D_3'} \frac{V_i}{R} \tag{49}$$

III. Calculation of Critical Inductance

In a dc-dc converter, boundary between performance of converter in CCM and DCM is determined by the critical inductance. Therefore, by measuring the value of critical inductance for L_1 (L_{C1}) and L_2 (L_{C2}) we can determine the operating mode of proposed converter. In critical mode, we get the following equation:

$$I_{LV1} + I_{LV2} = 0 \tag{50}$$

By applying the current-balancing law for capacitor C_o in CCM and considering $I_{LV2} = 0$, L_2 (L_{C2}) is obtained:

$$L_{C2} = \frac{D^2(1-D)R}{2f} = \frac{V_i DR}{2V_o f} \tag{51}$$

By applying the current-balancing law for capacitor C_1 in CCM, L_1 (L_{C1}) is obtained as follows:

$$L_{C1} = \frac{D^3(1-D)^2 R}{2f} = \frac{V_i^2 RD}{2V_o^2 f} \tag{52}$$

If the value of inductors is greater than the critical inductance, the converter is in CCM, and otherwise the converter operates in DCM.

IV. Calculation of Switching Stress

Peak current flow switch (PCFS) has a major role in converter design and reducing the cost of the converter. It can be reduced to minimum by proper selection of inductors. In following PCFS of the switches S_1 and S_2 are extracted.

A. Calculation of PCFS in CCM

The current of S_1 (i_{S1}) equals to:

$$i_{S1} = i_{L1} - i_{C1} = i_{L1} + i_{L2} \tag{53}$$

The PCFS of switch S_1 in CCM at $t = T_{on}$ (i_{SP1}^{CCM}) is:

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$$i_{SP1}^{CCM} = I_{LP1} + I_{LV2} = \frac{V_i}{2L_1}DT - \frac{V_i}{2L_2}T + \frac{V_o^2}{RV_i}D \quad (54)$$

By substituting (51) and (52) into (54), the maximum PCFS of S_1 in CCM ($i_{SP1,\max}^{CCM}$) is obtained as follows:

$$i_{SP1,\max}^{CCM} = \frac{2V_o^2}{RV_i} \quad (55)$$

The current of switch S_2 (i_{S2}) is:

$$i_{S2} = i_{L2} \quad (56)$$

The PCFS of switch S_2 at $t = T_{off}$ (i_{SP2}^{CCM}) is as follows:

$$i_{SP2}^{CCM} = I_{LP2} = \frac{V_i}{2L_2}T + \frac{I_o}{D} = I_o\left[\frac{D(1-D)R}{2L_2 f} + \frac{1}{D}\right] \quad (57)$$

By substituting (51) into (57), the maximum PCFS of switch S_2 in CCM ($i_{SP2,\max}^{CCM}$) is resulted as follows:

$$i_{SP2,\max}^{CCM} = \frac{2}{D}I_o \quad (58)$$

B. Calculation of PCFS in DCM

The current of switch S_1 equals to:

$$i_{S1} = i_{L1} + i_{C1} \quad (59)$$

The PCFS of switch S_1 in DCM (i_{SP1}^{DCM}) is obtained at $t = t_2$ as follows:

$$i_{SP1}^{DCM} = I_{LP1} \quad (60)$$

The current of switch S_2 is:

$$i_{S2} = i_{L2} \quad (61)$$

At $t = t_4$, the PCFS of switch S_2 in DCM (i_{SP2}^{DCM}) is:

$$i_{SP2}^{DCM} = I_{LP2} \quad (62)$$

V. Extended of Proposed Converter and Efficiency Calculation

According to Fig. 5, it is possible to construct n-stage boost converter by repeatedly adding $D_{2n} - D_{2n-1} - C_n - L_{n+1}$ $(n = 2,3,...)$ in proposed structure shown in Fig. 1. In proposed n-stage boost structure, only two switches with $(n+1)$ inductors, $(n+1)$ capacitors and $(2n+1)$ diodes are used. In CCM, when the switch S_1 is turned on and the switch S_2 is turned off, the D_o diode is directly biased and the D_1, D_2, …, D_n diodes are reversely biased. Also, the inductors L_2, L_3, …, L_{n+1} and capacitors C_1, C_2, …, C_n are in series connection, therefore their stored energy are decreased and the capacitor C_o is charged. The series connection of n-capacitors increase V_o. When the switch S_1 is turned off and the switch S_2 is turned on, the D_1, D_2, …, D_n diodes are directly biased and the D_o diode is reversely biased. Hence, the stored energy of the inductors L_2, L_3, …, L_{n+1} and capacitors C_1, C_2, …, C_n are gradually increased and the capacitor C_o is discharged. At (t_1, t_2) and (t_3, t_4) in DCM all of the diodes are reversely biased, then, the energy of capacitors remains constant. The voltage gain of generalized n-stage converter in CCM and DCM are, respectively:

$$\frac{V_o}{V_i} = -\frac{n}{D(1-D)} \quad (63)$$

$$\frac{V_o}{V_i} = -\frac{n(D_1' + D_2' + D_3')(D_1' + D_3' + D_4')}{D_1' D_3'} \quad (64)$$

The critical inductance value of L_{Cn} $(n = 2,\ 3,\ ...)$ is:

$$L_{Cn} = \frac{D^2(1-D)R}{2nf} = \frac{V_i DR}{2V_o f} \quad (65)$$

The critical inductance of L_{C1} is equal to:

$$L_{C1} = \frac{D^3(1-D)^2 R}{2n^2 f} = \frac{V_i^2 RD}{2V_o^2 f} \quad (66)$$

Also, the maximum PCFS of switch S_2 equals to:

$$i_{SP2,\max,n}^{CCM} = \frac{2n}{D}I_o = \frac{2V_o^2(1-D)}{RV_i} \quad (67)$$

Assuming, the current ripple of inductors and the voltage ripple of capacitors are neglected. So, the root-mean-square (RMS) relation of inductors is given as follows:

$$I_{L1} = I_i = -\frac{nI_o}{D(1-D)} \quad (68)$$

$$I_{Ln} = nI_o \quad (69)$$

Then, the losses of inductors are equal to [26]:

$$P_{L1} = r_{L1}I_{L1}^2 + (Kf^{\alpha}B_{ac}^{\beta}W_{tfe})(10^{-3}) \quad (70)$$

$$P_{Ln} = \sum_{N=1}^{n}\left[r_{LN}I_{LN}^2 + (Kf^{\alpha}B_{ac}^{\beta}W_{tfe})(10^{-3})\right] \quad (71)$$

The diodes RMS current relations are obtained as follows:

$$I_{D(2m-1)} = \sqrt{\frac{1}{T}\int_0^{(1-D)T}\left(\frac{I_i}{n}\right)^2 dt} = -\frac{I_o\sqrt{1-D}}{D(1-D)} \quad m = 1,2,...,2n-1 \quad (72)$$

$$I_{D(2n)} = \sqrt{\frac{1}{T}\int_0^{(1-D)T}\left(\frac{I_i}{2n}\right)^2 dt} = -\frac{I_o}{2D(1-D)} \quad (73)$$

$$I_{Do} = I_{Co} + I_o = I_{Ln} = nI_o \quad (74)$$

By neglecting turn off state losses in the diodes and defining Q_{rr} as reverse recovery energy of diode, the losses can be obtained as follows [27]:

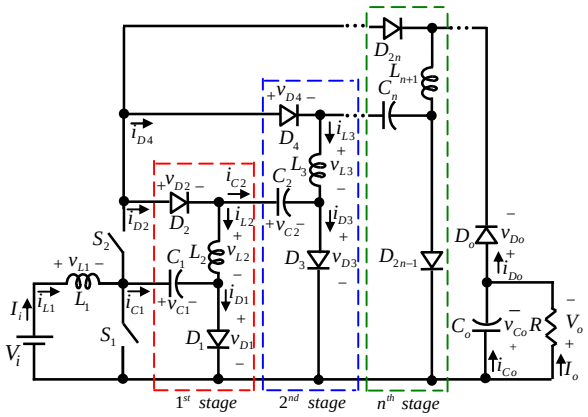

Fig. 5. Proposed converter for n-stage

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$$P_{D(2m-1)}=\sum_{M=1}^{2n-1}\left[V_F I_{D(2M-1),ave}+r_D I^2_{D(2M-1)}+\frac{Q_{rr}V_D f}{4}\right] \quad (75)$$

$$P_{D(2n)}=\sum_{N=1}^{n}\left[V_F I_{D(2N),ave}+r_D I^2_{D(2N)}+\frac{Q_{rr}V_D f}{4}\right] \quad (76)$$

$$P_{Do}=V_F I_{Do,ave}+r_D I^2_{Do}+\frac{Q_{rr}V_D f}{4} \quad (77)$$

The RMS values of C_n current are obtained as follows:

$$I_{Cn}=\sqrt{\frac{1}{T}\left[\int_0^{DT} I_o^2 dt+\int_0^{(1-D)T}\left(\frac{I_i}{2n}\right)^2 dt\right]}=I_o\sqrt{D+\frac{1}{4D^2(1-D)}} \quad (78)$$

By considering $Q^+_{Co}=Q^-_{Co}$, the RMS value of capacitor C_o current is equal to:

$$I_{Co}=\sqrt{\frac{1}{T}\left[\int_0^{DT}\left(I_o\frac{1-D}{D}\right)^2 dt+\int_0^{(1-D)T} I_o^2 dt\right]}=I_o\sqrt{\frac{(1-D)^2}{D}+(1-D)} \quad (79)$$

The losses of capacitors are calculated as follows:

$$P_{Cn}=\sum_{N=1}^{n} r_{CN} I^2_{CN} \quad (80)$$

$$P_{Co}=r_{Co} I^2_{Co} \quad (81)$$

The switches RMS current are equal to:

$$I_{S1}=\sqrt{\frac{1}{T}\int_0^{DT}(I_i+nI_o)^2 dt}=\sqrt{\frac{1}{T}\int_0^{DT}(I_i+nI_o)^2 dt} \quad (82)$$

$$I_{S2}=\sqrt{\frac{1}{T}\int_0^{(1-D)T}\left(\frac{2n-1}{2n}I_i\right)^2 dt}=\frac{2n-1}{2D(1-D)}I_o \quad (83)$$

By considering inter-electro capacitance of switch and free wheeling diode with $Q_{rr,BD}$ as reverse recovery energy, the below relations are obtained for switching losses [28]:

$$P_{S1}=r_{DS-on}I^2_{S1}+\frac{f}{2}(t_r+t_f)I_{S1,ave}V_{S1}+\frac{f}{2}C_{OSS}V^2_{S1}+\frac{fQ_{rr,BD}V_{S1}}{4}+r_{BD1,}I^2_{BD1}+V_{BF1}I_{BD1,ave} \quad (84)$$

$$P_{S2}=r_{DS-on}I^2_{S2}+\frac{f}{2}(t_r+t_f)I_{S2,ave}V_{S2}+\frac{f}{2}C_{OSS}V^2_{S2}+\frac{fQ_{rr,BD}V_{S2}}{4}+r_{BD2,}I^2_{BD2}+V_{BF2}I_{BD2,ave} \quad (85)$$

Thus, the total loss and efficiency are equal to:

$$P_{Loss}=P_{L1}+P_{Ln}+P_{S1}+P_{S2}+P_{Cn}+P_{Co}+P_{D(2m-1)}+P_{D(2n)}+P_{Do} \quad (86)$$

$$\eta\%=\frac{P_{out}}{P_{out}+P_{Loss}}\times 100 \quad (87)$$

From above relations, it can be noted that the losses increased and the efficiency reduced by increasing the switching frequency due to increased switching losses.

VI. Simulation and Experimental Results

In this section, simulation results in PSCAD/EMTDC and experimental results by using laboratory prototype are provided to prove the correctness of equations for the proposed converter shown in Fig. 5 and 1-stage. Parameters for the simulation and experimental results are given in Table II. Fig. 6 shows the scheme of the laboratory prototype which details of the elements are clearly visible.

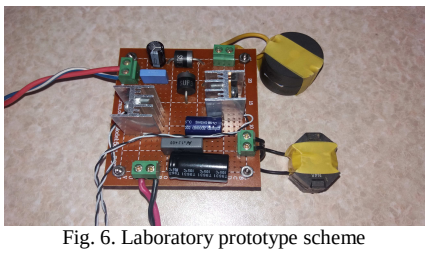

Fig. 6. Laboratory prototype scheme

TABLE II
ANALYSIS PARAMETERS FOR LABORATORY PROTOTYPE

Parameters	CCM	DCM
Duty cycle	$D=50\%$	$D'=50\%$
R	100Ω	
L_1	$L_1=2mH;\ r_{L1}=0.15\Omega$	$L_1=100\mu H;\ r_{L1}=0.005\Omega$
(Powder core)	$K=0.00551;\ \alpha=1.23;\ \beta=2.12;\ W_{tfe}=50.5;\ B_{ac}=0.0545$	
L_2	$L_2=4.5mH;\ r_{L2}=0.3\Omega$	$L_2=600\mu H;\ r_{L2}=0.007\Omega$
(Powder core)	$K=0.00551;\ \alpha=1.23;\ \beta=2.12;\ W_{tfe}=104.3;\ B_{ac}=0.0591$	
C_1	$68\mu F;\ r_{C1}=0.015\Omega$	
C_o	$47\mu F;\ r_{Co}=0.01\Omega$	
Diodes	Type: MUR1560; $V_{F,D}=0.8V;\ r_D=0.01\Omega$	
Switches N-channael MOSFET	Type: STW45NM50F; $r_{DS-on}=0.07\Omega;\ t_r=28nS;\ t_f=25nS$ $C_{OSS}=1260pF;\ Q_{rr}=1600nC;\ di/dt=100A/\mu S$	
V_i, f	$12V$, $10kHz$	

A. Critical Inductance Calculation

Considering the parameters shown in Table II, the values of L_{C1} and L_{C2} can be obtained as $156\mu H$ and $625\mu H$, respectively. By substituting L_{C1} and L_{C2}, the converter operates in critical mode and the current values of L_1 and L_2 achieved to zero.

B. Simulation and Experimental Results for CCM

Considering Table II, $L_1=2mH$ and $L_2=4.5mH$, the converter operates in CCM. Some simulation results in CCM are shown in Fig. 7. In accordance with the theoretical expression, the voltage of inductor L_1 in accordance with (1) is reached to $12V$ at T_{on} and in accordance with (2) is reduced and is achieved to $-12V$ at T_{off}. At T_{on}, the amount of inductor L_2 voltage is reduced gradually to $-24V$. At T_{off}, the voltage of inductor L_2 will be $24V$. The voltage variation of capacitor C_o is shown in Fig. 7(b). As shown, V_{Co} is approximately $48V$ that is confirmed (63). From Fig. 7(c), the current of switch S_1 at T_{on} is changed with (53) and its PCFS in accordance with (54) is reached to $3A$. At T_{off}, the current of switch S_1 is zero. In addition, the current of switch S_2 at T_{on} is equal to zero, and at T_{off}, it is changed in accordance with (56) and at $t=T_{off}$ is reached to its peak

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value $1A$ (eq. (57)). Also, the current of the diodes are shown in Fig. 7(d) which confirm (11) to (16).

The experimental results are provided to demonstrate the proposed converter operation in CCM (Figs. 8 and 9). As it can be seen, the experimental results reconfirm the theoretical analysis and simulation results with small difference due to parasitic elements. Substituting Table II into presented relations in section V yields $P_{L1}=0.5472W$, $P_{L2}=0.0685W$, $P_{C1}=0.085W$, $P_{Co}=0.00228W$, $P_{D1}=0.8324W$, $P_{D2}=0.4171W$, $P_{Do}=0.3846W$, $P_{S1}=0.2652W$ and $P_{S2}=0.0836W$. It should be noted that the third term of the diodes losses relations and fifth and sixth term of switch losses relations are neglected. Therefore, the total losses and calculated efficiency are $P_{Loss}=2.6858W$ and 89.5%, respectively. The experimental efficiency variation is shown in Fig. 9(h) for various duty ratios. As it can be seen, the proposed converter efficiency is improved by increasing D whereas the voltage gain is increased. Because, the parasitic elements of boosting circuit have lees turning on time. The experimental efficiency is almost 88% that is near to calculated value. The maximum measured efficiency of proposed converter is approximately 93.5% by considering Table II. It is clear that the maximum efficiency of the proposed converter is achieved around $D=0.93$. Other word, the voltage gain in this point is approximately 16. Also, the efficiency comparison of the proposed converter with [23] is shown in Fig. 8(h). Although, the proposed converter has more efficiency than [23] for lower D but the efficiency difference of the proposed converter and [23] is less for some higher D.

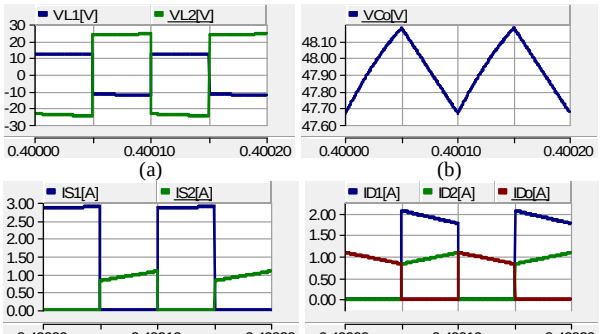
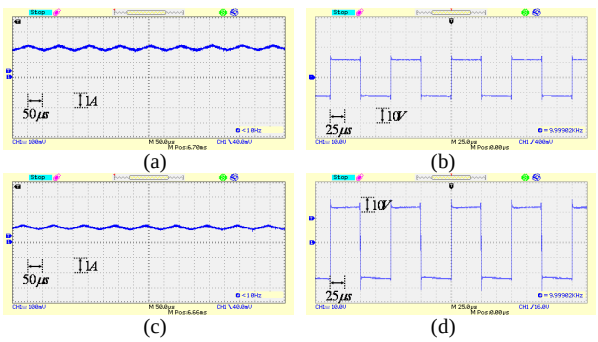


Fig. 7. Simulation results of proposed converter in CCM; (a) L_1 and L_2 voltages; (b) C_o voltage; (c) S_1 and S_2 current; (d) diodes current



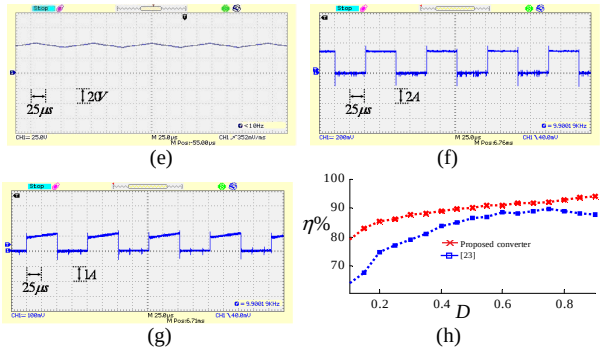


Fig. 8. Experimental results of proposed converter in CCM; (a) L_1 current; (b) L_1 voltage; (c) L_2 current; (d) L_2 voltage; (e) C_o voltage; (f) S_1 current; (g) S_2 current; (h) efficiency

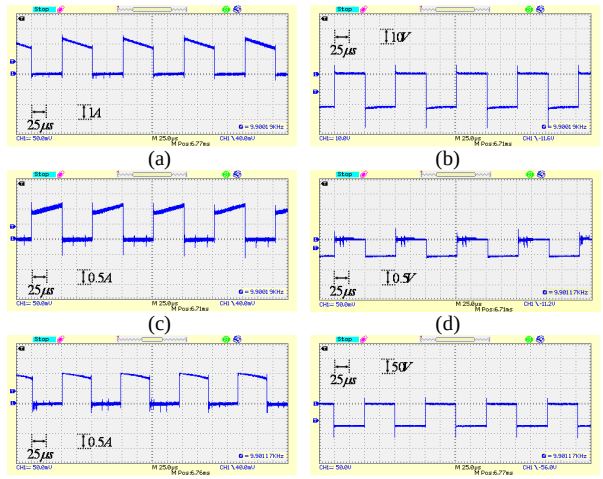


Fig. 9. Experimental results of proposed converter in CCM; (a) D_1 current; (b) D_1 voltage; (c) D_2 current; (d) D_2 voltage; (e) D_o current; (f) D_o voltage

C. *Simulation and Experimental Results for DCM*

Simulation results of the voltage of inductors L_1 and L_2 are carried out bearing in mind the parameters of Table II, $L_1=100\mu H$ and $L_2=600\mu H$ and its results in DCM is shown in Fig. 10(a). As can be seen, the voltage of inductor L_1 at $(t_0,\ t_2)$ in accordance with (19) is $12V$. At $(t_2,\ t_3)$, the voltage of inductor L_1 in accordance with (20) is gradually reduced and is reached to $-41V$. In addition, the voltage of inductor L_1 is zero at $(t_3,\ t_4)$. At $(t_0,\ t_1)$, the voltage of inductor L_2 is gradually reduced and at $t=t_1$ is zero. At $(t_1,\ t_2)$, the voltage of inductor L_2 is reached to zero. The voltage variation of capacitor C_o is shown in Fig. 10(b). As shown, V_{Co} in accordance with (64) is approximately $72V$. According to Fig. 10(c), the current of switch S_1 in accordance with (59) is changed and its peak current in accordance with (60) is equal to $8.5A$. In addition, the current of switch S_2 is equal in accordance with (61) and its peak current is $2.5A$ which confirms (62). Although some of the waveforms of the simulation results are presented in Fig. 10,

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but the experimental results for the validation of the circuit operation are fully presented in Figs. 11 and 12.

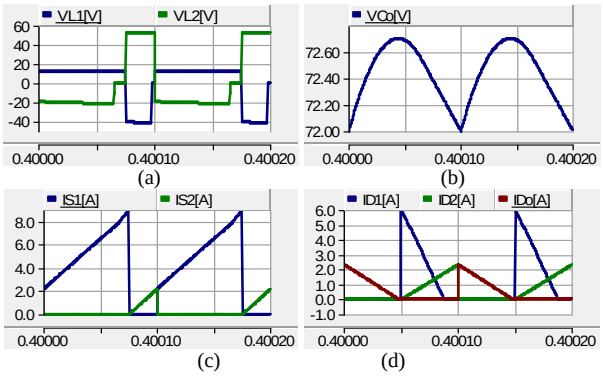

Fig. 10. Simulation results of proposed converter in DCM; (a) L_1 and L_2 voltages; (b) C_o voltage; (c) S_1 and S_2 current; (d) diodes current

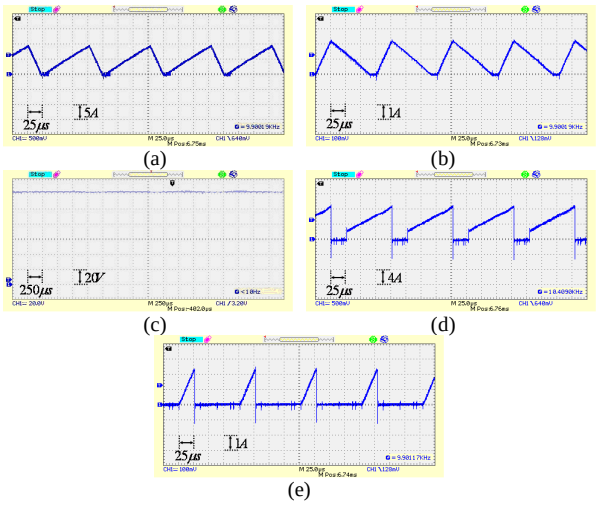

Fig. 11. Experimental results of proposed converter in DCM; (a) L_1 current; (b) L_2 current; (c) C_o voltage; (d) S_1 current; (e) S_2 current

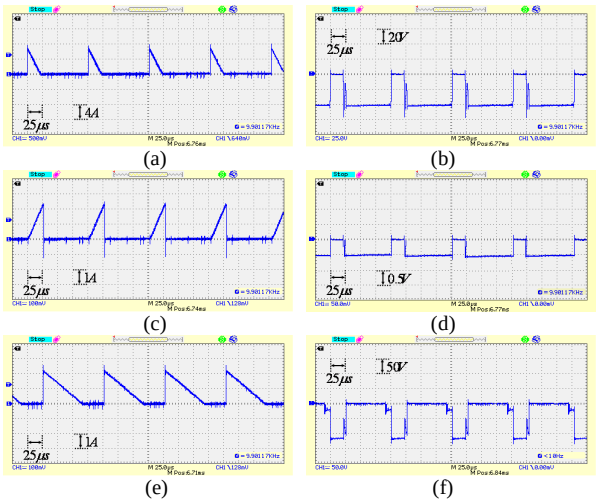

Fig. 12. Experimental results of proposed converter in DCM; (a) D_1 current; (b) D_1 voltage; (c) D_2 current; (d) D_2 voltage; (e) D_o current; (f) D_o voltage

As can be seen, the experimental results confirm the theoretical concepts and simulation results. It should be noted that there are differences between theoretical and experimental results due to parasitic components.

VII. Conclusion

In this paper, it was proposed a new structure for non-isolated dc-dc boost converters. The voltage and current equations of each elements and semiconductor devices were extracted in CCM and DCM, and the critical inductance relations were obtained for determine operating mode of the proposed converter. Meanwhile, the proposed converter features were presented by its development for n -stage with modular voltage boost circuit which can be cascaded for even higher voltage gain and its efficiency was calculated with more details. Finally, the presented theory was reaffirmed by simulation and experimental results for 1-stage converter. Also, the number of elements and switches of proposed converter were compared with other conventional boost converters based on SC and VL techniques and cascaded boost converter, and the voltage gain variations were analyzed by considering a same input voltage for various D . As a results, the proposed converter generates a proper voltage gain for the same input voltage and D . By considering $V_i = 12V$, $f = 10kHz$, $D = 50\%$ and $D' = 50\%$, the theoretical concepts and simulation results are confirmed by experimental results, fairly. As mentioned, the average output voltage is $48V$ and $72V$ in CCM and DCM, respectively. The PCFS of S_1 is $4A$ and $8.5A$ in CCM and DCM, respectively. Also, the PCFS of S_2 is $2A$ and $2.5A$ in CCM and DCM, respectively. The maximum proposed converter efficiency is reached nearly to 93.5%.

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